PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

TRANSMITTAL FOR A NEWLY EXECUTED ORIGINAL APPLICATION UNDER 37 C.F.R. §1.53(b)

This is a request for filing a patent application under 37 C.F.R. §1.53(b) for:

Inventor: Won Jun Lee

For: METAL THIN FILM OF SEMICONDUCTOR DEVICE AND METHOD FOR FORMING SAME

1. This is a new [X] **Utility** [ ] **Design** [ ] **Plant** patent application.

2. The papers enclosed to obtain a filing date are as follows:
   20 Pages of Specification including
   0 Title Page
   4 Pages of Claims
   1 Page of Abstract
   14 Sheets of drawings containing 31 Figures
   [ ] The enclosed drawing(s) are photograph(s), and there is also attached a PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)

3. Combined Declaration and Power of Attorney
   [X] Enclosed and is executed by all inventors.
   [ ] Not Enclosed.
   This application is being filed under the provisions of 37 C.F.R. §1.53(f). Applicant(s) await notification from the Patent and Trademark Office of the time set for filing the Declaration and paying the filing fees.

4. Language

[X] English

[ ] Non-English

This application is being filed in accordance with 37 C.F.R. §1.52(d) and §608.01 of the MPEP. Applicant(s) await notification from the Patent and Trademark Office of the time set for filing the verified English translation and the processing fee.

5. Assignment

[X] An assignment of the invention to Hyundai Electronics Industries Co., Ltd. and a PTO Form-1595, Recordation Form Cover Sheet, are enclosed.

[ ] An assignment will be filed at a later date.

6. Priority - foreign applications under 35 U.S.C. §119(a)-(d) or §365(b) or PCT international applications under 35 U.S.C. §365(a) designating at least one country other than the U.S.

[X] Priority of the following foreign application is claimed:

Country	Application No.	Filed
Korea	42158/2000	July 22, 2000

Certified copy: [X] is attached. [ ] will follow.

7. Priority based on provisional application(s) - 35 U.S.C. §119(e)

[ ] Priority of the following provisional application(s) is claimed:

Application No.	Filed

A. Relate Back - 35 U.S.C. §119(e)

[ ] Amend the specification by inserting before the first line the sentence: "This application claims priority of copending provisional application(s) No. _____ filed on _____."

8. Small entity status

[ ] A statement claiming small entity status under 37 C.F.R. §§1.9 and 1.27 is enclosed.

9. Fee Calculation (37 C.F.R. §1.16)

CLAIMS FOR FEE CALCULATION				
	Number Filed	Number Extra	at Rate of	Basic Fee Utility $710.00 Design $320.00
Total Claims (37 C.F.R. §1.16(c))	18 - 20 =		$ 18.00 each=	$0.00
Independent Claims (37 C.F.R. §1.16(b))	2 - 3 =		$ 80.00 each=	$0.00
Multiple dependent claim(s), if any (37 C.F.R. §1.16(d))			$270.00	+
			SUB-TOTAL =	**$710.00**
			Reduction by 1/2 for filing by a small entity	**- $**
			TOTAL FILING FEE =	**$710.00**

10. Fee Payment

[ ] Not Enclosed. **NO FEE IS BEING PAID BY CHECK OR DEPOSIT ACCOUNT AT THIS TIME.**
This application is being filed under the provisions of 37 C.F.R. §1.53(f). Applicant(s) await notification from the Patent and Trademark Office of the time set for filing the Declaration and paying the filing fees.

[X] Enclosed.

Two checks in the amounts of $710.00 and $40.00 representing the basic filing fee of $710.00 and an assignment recording fee of $40.00 are enclosed.

11. [X] **Except** for issue fees payable under 37 C.F.R. §1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account 50-0310. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. §1.136(a)(3).

12. Additional papers enclosed:

[X] Preliminary Amendment
[X] Information Disclosure Statement
[X] Form PTO-1449, 1 document included
[ ] Declaration of Biological Deposit
[ ] Submission of "Sequence Listing", computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.

Please accord this application an application number and filing date.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

William O. Trousdell

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Dated: November 22, 2000

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PATENT
Attorney Docket No. 041501-5411

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Won Jun LEE	)	
	)	
Application No.: Unassigned	)	Group Art Unit: Unassigned
	)	
Filed: November 22, 2000	)	Examiner: Unassigned
	)	

For: METAL THIN FILM OF SEMICONDUCTOR DEVICE AND METHOD FOR FORMING SAME

Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the examination of the above-identified application on the merits, please amend the application as follows:

IN THE BRIEF DESCRIPTION OF THE DRAWINGS:

Page 8, line 8, replace "Figs. 6a to 6d are sectional views" with --Fig. 6 is a sectional view--,

Page 8, line 10, replace "Figs. 7a to 7d" with --Figs. 7a to 7b--,

Page 9, line 20, replace "Figs. 6a to 6d are sectional views" with --Fig. 6 is a sectional view--,

Page 10, line 1, replace "Fig. 6a" with --Fig. 6 --,

Page 10, line 5, replace "Fig. 6b" with --Fig. 6 --,

Page 10, line 9, replace "Fig. 6c" with --Fig. 6 --,

Page 11, line 7, replace "Fig. 6d" with --Fig. 6 -- and

Page 13, line 5, replace "Figs. 7a to 7d" with -- Figs. 7a to 7b--.

REMARKS

Applicant respectfully submits that no new matter has been introduced by this Preliminary Amendment which is being made to place the application in better condition for examination.

If there is any fee due in connection with the filing of this Preliminary Amendment, please charge the fees to our Deposit Account No. 50-0310.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

By: William O. Trousdell
William O. Trousdell
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METAL THIN FILM OF SEMICONDUCTOR DEVICE AND METHOD FOR FORMING SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, and more particularly, to a metal thin film of a semiconductor device and method for forming the same in which excellent step coverage and surface roughness are maintained.

2. Background of the Related Art

Generally, a method for forming a metal line of a semiconductor device includes two processes such as a tungsten plug + reactive ion etching (RIE) Al process and an Al plug process. In the tungsten plug process, it is possible to even fill a relatively small sized via so as to improve reliability. However, in this case, process steps are relatively complicate and the production cost is high. On the other hand, the Al plug process has advantages that process steps are simple and the production cost is low, but there is a problem that it is difficult for the Al plug process to apply to a microdevice of high packing density.

A related art metal thin film and method for forming a metal line using the same will be described below.

First, a process for forming a metal line using tungsten plug will be described.

Figs. 1a to 1e are sectional views of a related art process for forming a metal line using tungsten plug.

As shown in Fig. 1a, an interleaving insulating film 2 is formed on a semiconductor substrate 1 and then selectively etched to form a contact hole 3.

Subsequently, as shown in Fig. 1b, a thin barrier metal layer 4 is formed on an entire surface of the semiconductor substrate 1 including the contact hole 3.

As shown in Fig. 1c, blanket tungsten W is deposited on the contact hole 3 on which the barrier metal layer 4 is formed, by chemical vapor deposition (CVD) process to completely fill the contact hole 3. Thus, a material layer for the formation of plug, i.e., a tungsten layer 5 is formed. At this time, the tungsten layer 5 fills the contact hole 3 and is also formed on the interleaving insulating film 2.

Afterwards, as shown in Fig. 1d, the tungsten layer 5 is planarized by chemical mechanical polishing (CMP) process or etch-back process to form a plug layer 5a.

Finally, as shown in Fig. 1e, an anti-reflective coating (ATC) layer 6 and an Al layer 7 are deposited on the entire surface on which the plug layer 5a is formed. Thus, a metal line is formed.

The aforementioned process for forming a metal line using tungsten plug has advantages that currently used equipments are used as they are and that the process technology tested and verified by actual mass production is used. However, the production cost is high ($14.36/wf) and a lot of process steps are required, thereby reducing yield. Also, since blanket deposition process is used, it is likely that void occurs if the size of the contact hole becomes smaller.

Now, a process for forming a metal line using Al reflow will be described.

Figs. 2a to 2d are sectional views of a related art process for forming a metal line using Al reflow.

As shown in Fig. 2a, an interleaving insulating film 22 is formed on a semiconductor substrate 21 and then selectively etched to form a contact hole 23. The contact hole 23 has a wine glass type of which corner portions are rounded, so as to improve filling efficiency of a material for the formation of plug.

Subsequently, as shown in Fig. 2b, a barrier layer and a wetting layer 24 are formed on a surface of the interleaving insulating film 22 including bottom and wall of the contact hole 23. As shown in Fig. 2c, an Al layer 25 is formed by physical vapor deposition (PVD) process. At this time, the Al layer 25 does not completely fill the contact hole 23 but partially fills the contact hole 23 due to characteristic of the PVD process.

Afterwards, as shown in Fig. 2d, the Al layer 25 is reflowed by annealing process at a temperature of 550°C or greater, and then is planarized to completely fill the contact hole 23. Thus, a metal line layer 25a of plug + main line structure is formed.

The aforementioned process for forming a metal line using Al reflow has an advantage that the production cost is low. However, there are problems that additional process for forming a contact hole having a shape capable of being filled is required, and aspect ratio of the contact hole is limited. Also, there are still problems that high temperature and low vacuum equipment is required, and line resistance may increase due to high temperature process.

Another related art method for forming a metal line using Al cold-hot deposition will be described with reference to Figs. 3a to 3d.

Figs. 3a to 3d are sectional views of a related art process for forming a metal line using Al cold-hot deposition.

As shown in Fig. 3a, an interleaving insulating film 32 is formed on a semiconductor substrate 31 and then selectively etched to form a contact hole 33. The contact hole 33 has a greater top width than a bottom width, so as to improve filling efficiency of a material for the formation of plug.

Subsequently, as shown in Fig. 3b, a barrier layer and a wetting layer 34 are formed on a surface of the interleaving insulating film 32 including bottom and wall of the contact hole 33. As shown in Fig. 3c, a cold Al layer 35 is formed on the barrier layer and the wetting layer 34.

Afterwards, as shown in Fig. 3d, a hot Al layer 35a is formed at a temperature of 400~550°C to form a metal line layer of plug + main line structure.

The aforementioned process for forming a metal line using Al cold-hot deposition has advantages that no additional equipment is required because the number of process steps is small and thus the production cost is low. However, there is a problem that aspect ratio of the contact hole is limited. Also, there is a problem that line resistance may increase because relatively high temperature process is required.

Another related art method for forming a metal line using CVD/PVD Al will be described with reference to Figs. 4a to 4d.

Figs. 4a to 4d are sectional views of a related art process for forming a metal line using CVD/PVD Al.

As shown in Fig. 4a, an interleaving insulating film 42 is formed on a semiconductor substrate 41 and then selectively etched by Ar sputtering process to form a contact hole 43.

Subsequently, as shown in Fig. 4b, a barrier layer and a nucleation layer 44 are formed on an upper surface of the interleaving insulating film 42 including bottom and wall of the contact hole 43. The barrier layer is formed by depositing Ti, TiN or Ti/TiN by ionized PVD or CVD process.

As shown in Fig. 4c, a CVD Al layer 45 is formed on an entire surface on which the barrier layer and the wetting layer 44 are formed, at a thickness of 1000Å or less by CVD process.

Afterwards, as shown in Fig. 4d, a PVD Al layer 46 is formed on the CVD Al layer 45 by performing PVD process at a temperature of 350~400°C to form a plug layer and a main line layer. The CVD Al layer 45 is used as the wetting layer required for reflow of the PVD Al layer 46. Al is deposited on the CVD Al layer 45 at a relatively high temperature and low power of 5kW or less by PVD process, so that reflow occurs.

To improve accuracy of a subsequent patterning process, an ARC layer may be formed on the PVD Al layer 46. Ti/TiN may be used as the ARC layer.

IMP Ti/MOCVD TiN is mainly used as a metal for forming the barrier layer during the PVD/CVD Al line process, due to its excellent via filling characteristic.

The metal deposition by CVD process used in the process for forming a metal line has more excellent via filling characteristic than the PVD reflow and thus many researches using CVD have progressed in Al plug process of a next generation device. Particularly, deposition

speed of the aforementioned process using PVD/CVD Al is higher than deposition speed by CVD process only, and an alloying element can be added so that a metal line having high productivity and high reliability can be fabricated. However, there is a problem that IMP Ti/MOCVD TiN mainly used as the barrier metal due to excellent via filling characteristic has a poor surface texture of a metal thin film closely related to electromigration resistance, and for this reason, reliability of the metal line is not better than IMP Ti.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a metal thin film of a semiconductor device and method for forming the same that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a metal thin film of a semiconductor device and method for forming the same in which excellent step coverage and surface roughness are maintained.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a metal thin film of a semiconductor

device according to the present invention includes: a barrier metal layer formed on a semiconductor substrate; and a PVD seed thin film, a CVD thin film, and a PVD reflow thin film sequentially formed on the barrier metal layer, wherein the PVD seed thin film, the CVD thin film and the PVD reflow thin film are of the same material.

In another aspect, a method for forming a metal thin film of a semiconductor device according to the present invention includes the steps of: forming an interleaving insulating film on a semiconductor substrate and selectively etching the interleaving insulating film to form a contact hole; forming a barrier metal layer on the interleaving insulating film including the contact hole; forming a PVD seed thin film on the barrier metal layer; forming a CVD thin film on the PVD seed thin film; and forming a PVD reflow thin film on the CVD thin film to fill the contact hole and form a flat thin film on the interleaving insulating film.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figs. 1a to 1e are sectional views of a related art process for forming a metal line using tungsten plug;

Figs. 2a to 2d are sectional views of a related art process for forming a metal line using Al reflow;

Figs. 3a to 3d are sectional views of a related art process for forming a metal line using Al cold-hot deposition;

Figs. 4a to 4d are sectional views of a related art process for forming a metal line using CVD/PVD Al;

Fig. 5 is a sectional view of a metal thin film according to the present invention;

Figs. 6a to 6d are sectional views of a process for forming the metal thin film according to the present invention;

Figs. 7a to 7d show characteristic graphs showing reflection factor and surface roughness of a CVD/PVD Al thin film according to a barrier metal;

Figs. 8a to 8d are AFM images showing surface morphologies of the CVD/PVD Al thin film according to the barrier metal;

Figs. 9a and 9b are XRD pattern and rocking curve of the CVD/PVD Al thin film according to the barrier metal; and

Figs. 10a to 10d are graphs showing via filling characteristic of a CVD/PVD Al process according to the barrier metal.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Fig. 5 is a sectional view of a metal thin film according to the present invention.

A metal thin film according to the present invention includes a barrier metal layer 52 formed on a semiconductor substrate 51 including an interleaving insulating film (not shown), and a PVD seed thin film 53, a CVD thin film 54, and a PVD reflow thin film 65 sequentially formed on the barrier metal layer 52. The barrier metal layer 52 is of Ti, TiN or Ti/TiN, wherein Ti is formed by IMP process and TiN is formed by metal-organic chemical vapor deposition (MOCVD) process. Also, the barrier metal layer 52 may be of IMP Ti or IMP Ti/TiN. The PVD seed thin film 53, the CVD thin film 54 and the PVD reflow thin film 65 are of the same material such as Al or Cu.

The aforementioned metal thin film according to the present invention can allow nuclei formation of the CVD thin film 54 and improve its fine structure by depositing the PVD seed thin film 53 between the barrier metal layer 52 and the CVD thin film 54. In other words, to solve problems related to nuclei formation and fine structure of Al, an Al<111> thin film useful for nuclei formation and growth of CVD Al is formed as a seed layer by PVD process, and then a later process is formed.

Meanwhile, an ARC layer of Ti/TiN may further be formed on the PVD reflow thin film 55.

A method for forming the aforementioned thin film according to the present invention will be described below.

Figs. 6a to 6d are sectional views of a process for forming the metal thin film according to the present invention.

As shown in Fig. 6a, a barrier metal layer 62 is formed on a semiconductor substrate 61 in which an interleaving insulating film (oxide film) including a contact hole in a particular portion is formed. To ensure cleanness of the contact hole, cleaning process is performed using plasma before the barrier metal layer 62 is formed.

As shown in Fig. 6b, a process for forming a plug layer is performed. Namely, a PVD seed thin film 63 is formed on the barrier metal layer 62 as a seed layer. The PVD seed thin film 63 is formed of Al or Cu with a thickness of 2000Å or less at a low temperature of 300°C or less and high power of 5kW or greater.

Subsequently, as shown in Fig. 6c, a CVD thin film 64 is formed on the PVD seed thin film 63 at a thickness of 1000Å or less. The CVD thin film 64 is of Al, and an organic metal compound, such as dimethyl aluminum hydride (DMAH), $(CH_3)_2AlH$, dimethyl ethyl amine alane (DMEAA) and $AlH_3N(CH_3)_2(C_2H_5)$), or a blend material containing the organic metal compound is used as a precursor of the CVD thin film 64.

The CVD thin film 64 may be formed at a deposition temperature of 150~300°C and a deposition pressure of 1~100Torr using a blend material in which adduct of a small amount is added to DMAH.

In case where the CVD thin film 64 is of Cu, Lewis-base stabilized Cu(I)beta-diketonate or a blend material containing it is used as a precursor. The CVD thin film 64 may be formed at a deposition temperature of 100~300°C and a deposition pressure of 1~100Torr using a blend material in which tmvs and Hhfac Dihydrate (HDH) are added to Cu(hfac)(tmvs) as a blend precursor.

In case where the CVD thin film 64 is formed of Al, the barrier metal layer 62 is formed of Ti, TiN, or Ti/TiN, wherein Ti is deposited by ionized PVD process and TiN is deposited by ionized PVD or CVD process. In case where the CVD thin film 64 is formed of Cu, the barrier metal layer 62 is formed of Ta, TaN, Ta/TaN, TiN, Ti/TiN or Wnx, wherein Ta and Ti are deposited by ionized PVD process while Tan, TiN and Wnx are deposited by ionized PVD or CVD process.

As shown in Fig. 6d, a PVD reflow thin film 65 is formed on the CVD thin film 64. At this time, in case where the PVD reflow thin film 65 is formed of Al, a deposition process is performed at a temperature of 300°C or greater (preferably, 350~400°C) and power of 5kW or less or power of 5kW or greater. Then, a subsequent annealing process is performed. Alternatively, high power of 5kW or greater and low power of 5kW or less are used in turn.

In case where the PVD reflow thin film 65 is formed of Cu, a deposition process is performed at a temperature of 300°C or greater (preferably, 350~400°C) and power of 5kW or less or power of 5kW or greater. Then, a subsequent annealing process is performed. Alternatively, high power of 5kW or greater and low power of 5kW or less are used in turn.

The PVD reflow thin film 65 has a thickness less than 50% of the final thickness of the overall thin films.

Additionally, to improve accuracy of a subsequent patterning process, an ARC layer of Ti/TiN may be formed on the PVD reflow thin film 65.

In the aforementioned method for forming a metal thin film according to the present invention, the CVD thin film is deposited on the PVD seed thin film so as to improve nuclei

formation and fine structure as compare with the case where the CVD thin film is deposited on the barrier metal layer.

When forming the CVD thin film, DMAH, $(CH_3)_2AlH$, DMEAA and $AlH_3N(CH_3)_2(C_2H_5)$) which may be used as a precursor have selectivity in which deposition speed is high on a conductive substrate such as metal while deposition does not almost occur on a nonconductive substrate such as oxide film.

In case of a metal substrate, of course, growth speed and fine structure of the CVD thin film may be varied depending on kinds of metal and process conditions.

In view of reliability of a metal line, the most preferred metal line fine structure is a thin film uniformly aligned in <111> direction and thus it is important to select a substrate which allows the CVD thin film to be aligned in <111> direction.

Generally, in case of PVD Al, a Ti thin film aligned in <002> direction is known as the most excellent barrier metal layer in view of alignment of Al thin film. Ti<002>/TiN<111> thin film is also known as an excellent barrier metal layer. Nonetheless, it is difficult to obtain excellent nuclei formation and alignment characteristic

equivalent to the case where the CVD thin film is formed on the PVD thin film of the same material as the CVD film.

Particularly, the method for forming a metal thin film according to the present invention has advantages that, in even case where IMP Ti/MOCVD TiN barrier known as the barrier metal layer having the most excellent Al filling characteristic is used, problems related to Al

nuclei formation and fine structure can be solved by forming the IMP Ti/MOCVD TiN barrier on the PVD seed thin film.

Characteristics of CVD/PVD Al thin film for both IMP Ti and IMP Ti/MOCVD TiN barrier will be described below.

Figs. 7a to 7d show characteristic graphs showing reflection factor and surface roughness of a CVD/PVD Al thin film according to a barrier metal.

Referring to Figs. 7a and 7b, in reflection factor and surface roughness of the CVD/PVD Al thin film, it is noted that reflection factor is lower and surface roughness is greater on the Ti/TiN barrier than the Ti barrier when the PVD Al seed is not applied. However, in case where the PVD seed thin film is applied in the same manner as the present invention, it is noted that reflection factor and surface roughness are improved in case of both the Ti and Ti/TiN barriers. Particularly, it is noted that reflection factor and surface roughness are improved in case of Ti/TiN barrier.

In Fig. 7a and 7b, Ti denotes IMP Ti, Ti/TiN denotes IMP Ti/MOCVD TiN, and seed denotes PVD Al seed layer.

Figs. 8a to 8d are AFM images showing surface morphologies of the CVD/PVD Al thin film according to the barrier metal.

Referring to Figs. 8a to 8d, it is noted that a surface morphology becomes smooth in case where the PVD see thin film is used. Particularly, it is noted that a surface morphology remarkably becomes smooth in case where the Ti/TiN barrier is used and the PVD Al seed layer of the present invention is formed.

In more detail, Fig. 8a shows a surface morphology of the CVD/PVD Al thin film in case of IMP Ti barrier, Fig. 8b shows a surface morphology of the CVD/PVD Al thin film in case of IMP Ti/MOCVD TiN barrier, Fig. 8c shows a surface morphology of the Al thin film in case of IMP Ti barrier and PVD Al seed layer, and Fig. 8d shows a surface morphology of Al thin film in case of IMP Ti/MOCVD TiN barrier and the PVD Al seed layer.

Figs. 9a and 9b show XRD patterns obtained by each sample. Referring to Figs. 9a and 9b, it is noted that Theta-2theta scan and Al<111> rocking curve show excellent <111> surface texture in Ti rather than Ti/TiN. It is also noted that a surface texture of the Al thin film becomes excellent by the PVD Al seed layer.

Figs. 10a to 10d are graphs showing via filling characteristic through via distribution. Referring to Figs. 10a to 10d, four samples of thin films are applied to Al plug formation process of two-level metallization process and thus via resistance distribution is obtained.

Fig. 10a shows via filling characteristic in case where IMP Ti is used as the barrier metal, and Fig 10b shows via filling characteristic in case where IMP Ti/MOCVD TiN is used as the barrier metal.

Fig. 10c shows via filling characteristic in case where IMP Ti is used as the barrier metal and the PVD Al seed layer is applied, and Fig. 10d shows via filling characteristic in case where IMP Ti/MOCVD TiN is used as the barrier metal and the PVD Al seed layer is applied.

It is noted that surface roughness of the Al thin film and <111> alignment characteristics can be improved without affecting Al filling characteristic in Ti/TiN substrate. It is also noted that surface roughness of the Al thin film, <111> alignment characteristics, and

Al filling characteristic can be improved without affecting Al filling characteristic in a Ti/TiN substrate.

When forming the plug layer and the main line layer using the metal thin film, it doesn't matter whichever contact hole is used. Particularly, even if the contact hole is formed to have a vertical structure having an upper portion and a lower portion of the same width, it is possible to fulfill all the conditions of the metal line.

As aforementioned, the metal thin film and method for forming the same according to the present invention has the following advantages.

Since the barrier metal layer having the excellent via filling characteristic is used, electromigration characteristic can be improved. Furthermore, since excellent step coverage and surface roughness can be maintained, reliability of wiring can be improved.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.

WHAT IS CLAIMED IS:

1. A metal thin film of a semiconductor device comprising:

a barrier metal layer formed on a semiconductor substrate; and

a PVD seed thin film, a CVD thin film, and a PVD reflow thin film sequentially formed on the barrier metal layer, wherein the PVD seed thin film, the CVD thin film and the PVD reflow thin film are of the same material.

2. The metal thin film of claim 1, the PVD seed thin film, the CVD thin film, and the PVD reflow thin film are of Al or Cu.

3. The metal thin film of claim 1, further comprising an interleaving insulating film between the semiconductor substrate and the PVD seed thin film.

4. The metal thin film of claim 1, wherein the barrier metal layer is of any one of Ti, TiN and Ti/TiN.

5. The metal thin film of claim 1, further comprising an ARC layer of Ti/TiN on the PVD reflow thin film.

6. A method for forming a metal thin film of a semiconductor device comprising the steps of:

forming an interleaving insulating film on a semiconductor substrate and selectively etching the interleaving insulating film to form a contact hole;

forming a barrier metal layer on the interleaving insulating film including the contact hole;

forming a PVD seed thin film on the barrier metal layer;

forming a CVD thin film on the PVD seed thin film; and

forming a PVD reflow thin film on the CVD thin film to fill the contact hole and form a flat thin film on the interleaving insulating film.

7. The method of claim 6, further comprising the step of cleaning an internal portion of the contact hole and a surface of the interleaving insulating film by cleaning process using plasma.

8. The method of claim 6, wherein the PVD seed thin film, the CVD thin film and the PVD reflow thin film are of the same material.

9. The method of claim 6, wherein the PVD seed thin film is formed of Al or Cu with a thickness of 2000Å or less at a low temperature of 300°C or less and high power of 5kW or greater.

10. The method of claim 6, wherein the CVD thin film is formed at a thickness of 1000Å or less, and in case where the CVD thin film is of Al, an organic metal compound, such as dimethyl aluminum hydride (DMAH), $(CH_3)_2AlH$, dimethyl ethyl amine alane (DMEAA) and $AlH_3N(CH_3)_2(C_2H_5)$), or a blend material containing the organic metal compound is used as a precursor.

11. The method of claim 10, wherein the CVD thin film is formed at a deposition temperature of 150~300°C and a deposition pressure of 1~100Torr using a blend material in which adduct of a small amount is added to DMAH.

12. The method of claim 6, wherein the CVD thin film is formed at a thickness of 1000Å or less, and in case where the CVD thin film is of Cu, Lewis-base stabilized Cu(I)beta-diketonate or a blend material containing it is used as a precursor.

13. The method of claim 12, wherein the CVD thin film is formed at a deposition temperature of 100~300°C and a deposition pressure of 1~100Torr using a blend material in which tmvs and Hhfac Dihydrate (HDH) are added to Cu(hfac)(tmvs) as a blend precursor.

14. The method of claim 6, wherein, in case where the CVD thin film is formed of Al, the barrier metal layer is formed of Ti, TiN, or Ti/TiN, where Ti is deposited by ionized PVD process and TiN is deposited by ionized PVD or CVD process.

15. The method of claim 6, wherein, in case where the CVD thin film is formed of Cu, the barrier metal layer is formed of either any one of Ta, TaN, Ta/TaN, TiN, and Ti/TiN or Wnx, where Ta and Ti are deposited by ionized PVD process while Tan, TiN and Wnx are deposited by ionized PVD or CVD process.

16. The method of claim 6, wherein the PVD reflow thin film has a thickness less than 50% of the final thickness of the completed thin films.

17. The method of claim 6, wherein the PVD reflow thin film is formed by a deposition process performed at a temperature of 300°C or greater and power of 5kW or less or power of 5kW or greater so as to perform a subsequent annealing process, or by a deposition process performed using high power (5kW or greater) and low power (5kW or less) in turn.

18. The method of claim 6, further comprising an ARC layer of Ti/TiN on the PVD reflow thin film.

ABSTRACT OF THE DISCLOSURE

A metal thin film of a semiconductor device and method for forming the same is disclosed, in which excellent step coverage and surface roughness are maintained. The metal thin film of a semiconductor device according to the present invention includes: a barrier metal layer formed on a semiconductor substrate; and a PVD seed thin film, a CVD thin film, and a PVD reflow thin film sequentially formed on the barrier metal layer, wherein the PVD seed thin film, the CVD thin film and the PVD reflow thin film are of the same material.

FIG.1a
related art

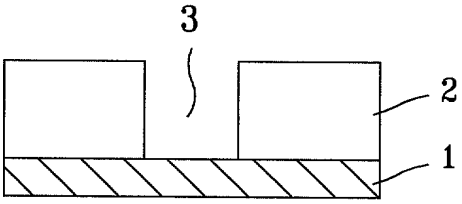


FIG.1b
related art

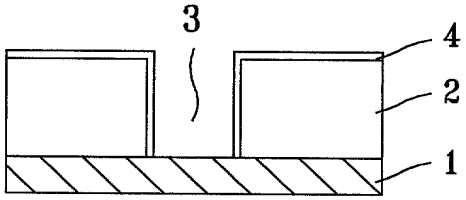


FIG.1c
related art

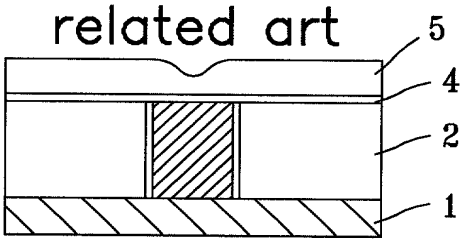


FIG.1d
related art

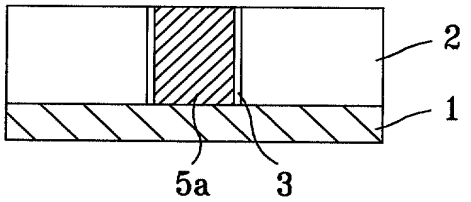


FIG.1e
related art

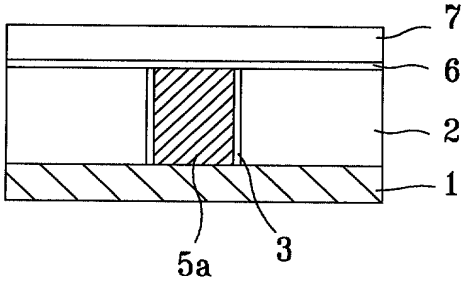


FIG.2a
related art

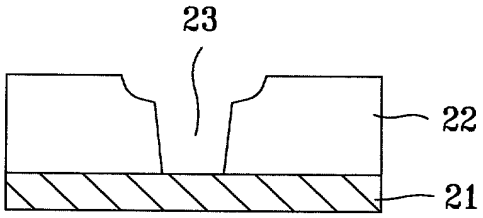


FIG.2b
related art

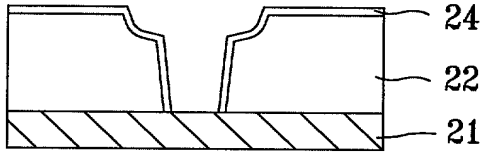


FIG.2c
related art

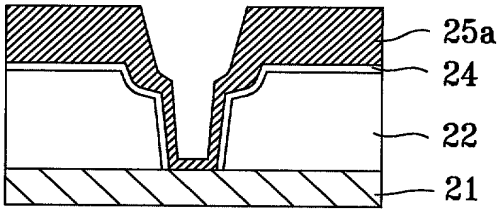


FIG.2d
related art

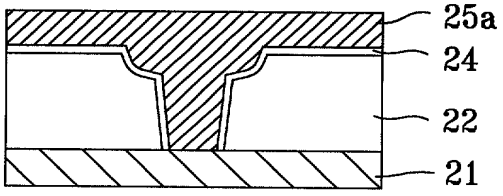


FIG.3a
related art

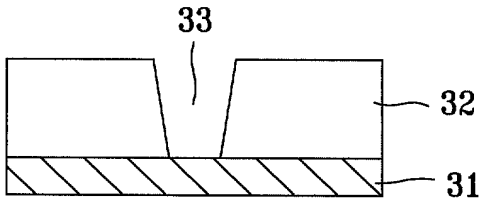


FIG.3b
related art

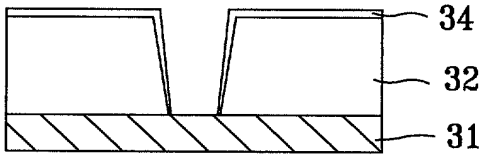


FIG.3c
related art

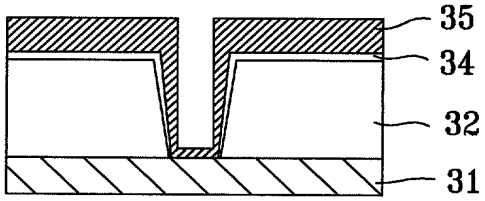


FIG.3d
related art

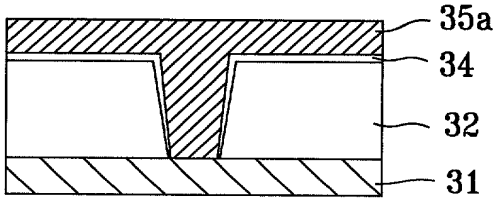


FIG.4a
related art

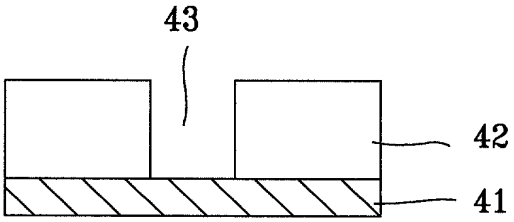


FIG.4b
related art

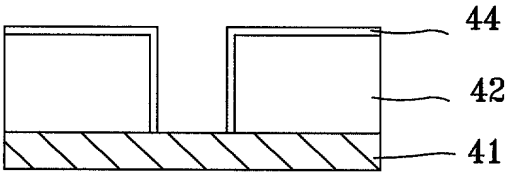


FIG.4c
related art

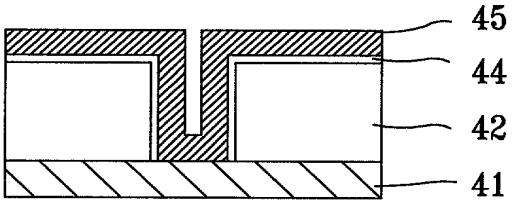


FIG.4d
related art

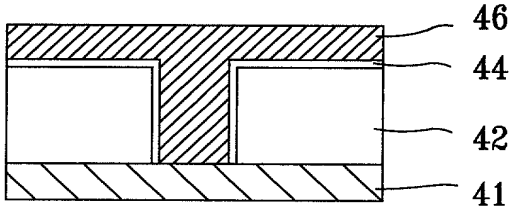


FIG.5

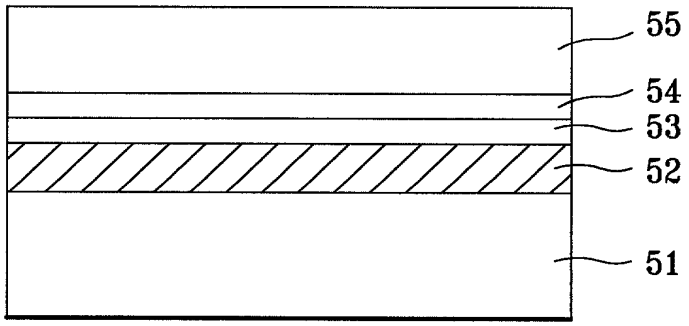


FIG.6

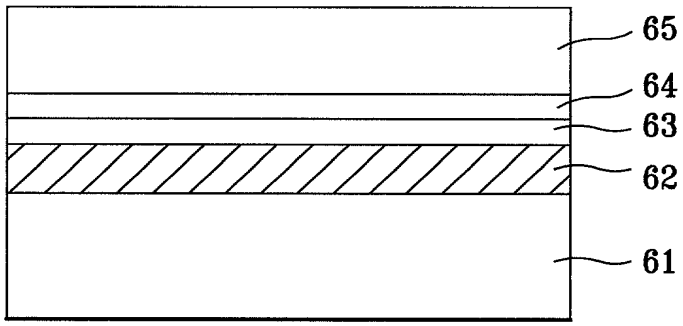
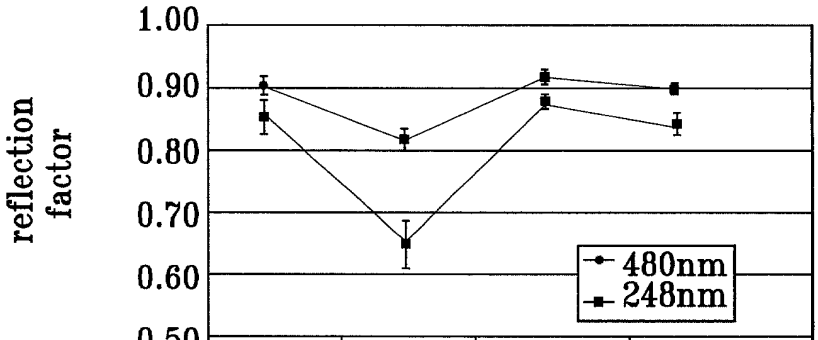
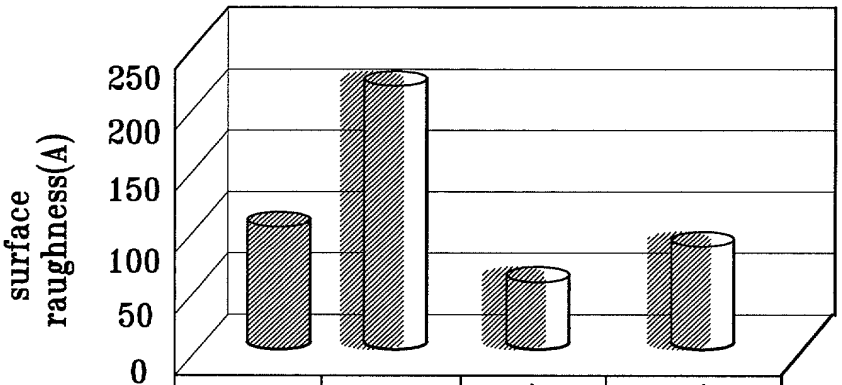


FIG.7a



	Ti	TiN	Tiw/seed	TiN w/seed
480nm	0.8974	0.8100	0.9094	0.9010
248nm	0.8401	0.6294	0.8813	0.8513

FIG.7b



	Ti	TiN	Tiw/seed	TiNw/seed
RMS	85	209	44.1	68.5

FIG.8a

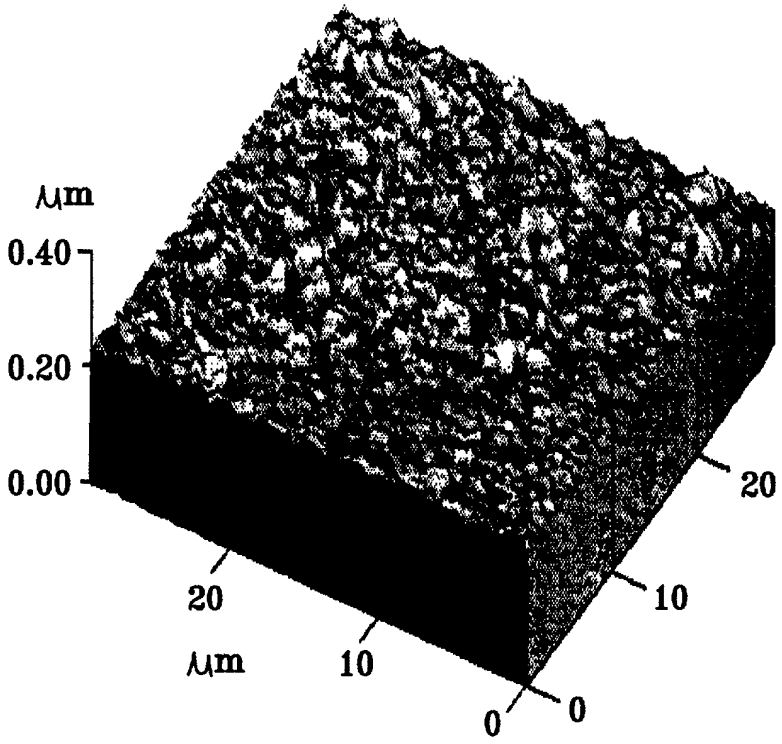


FIG.8b

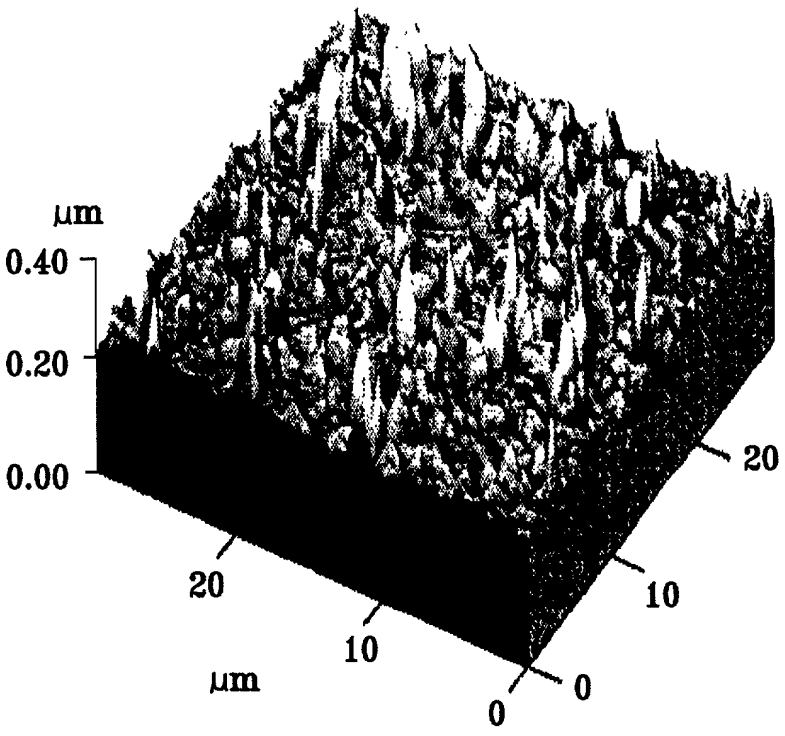


FIG.8c

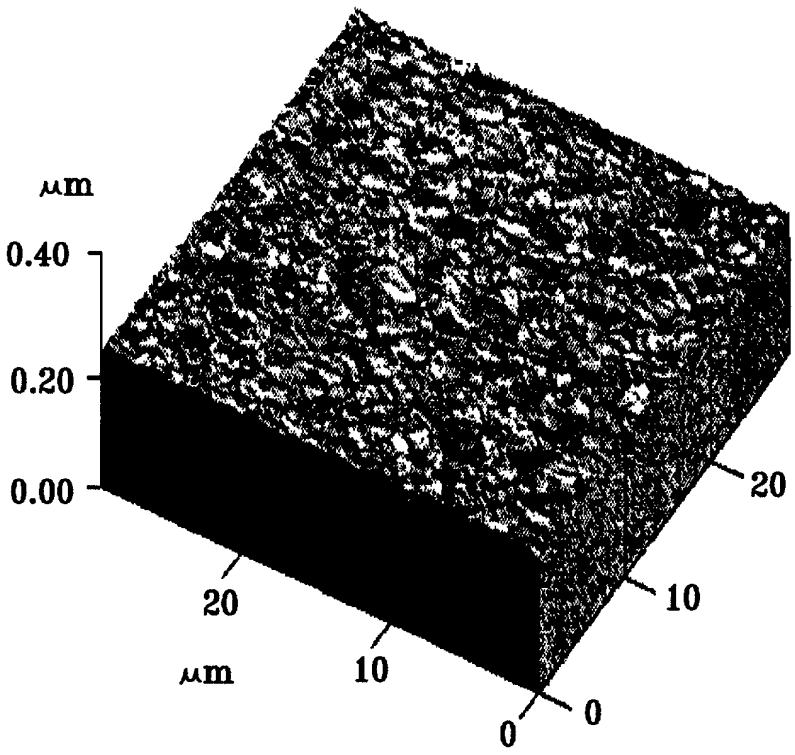


FIG.8d

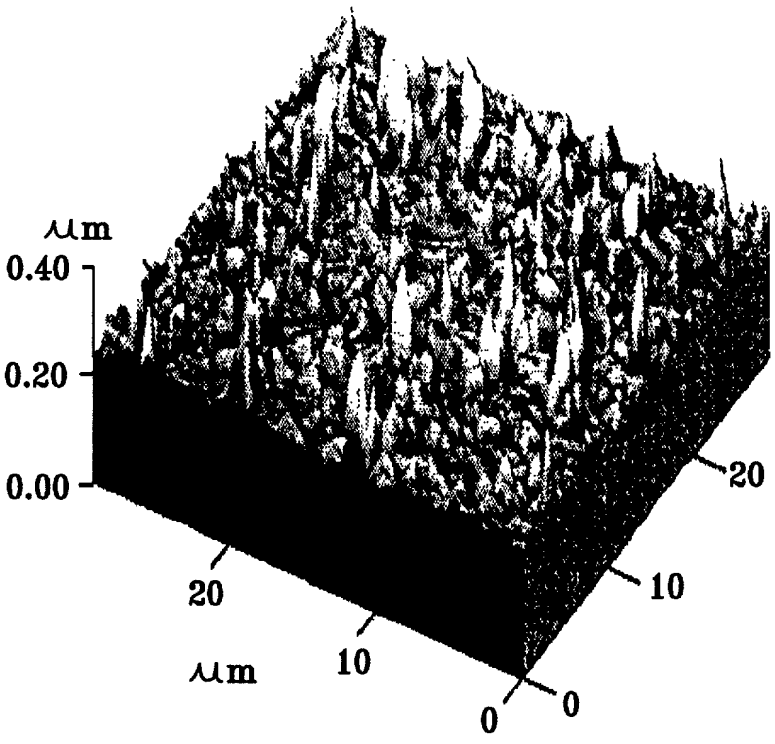


FIG.9a

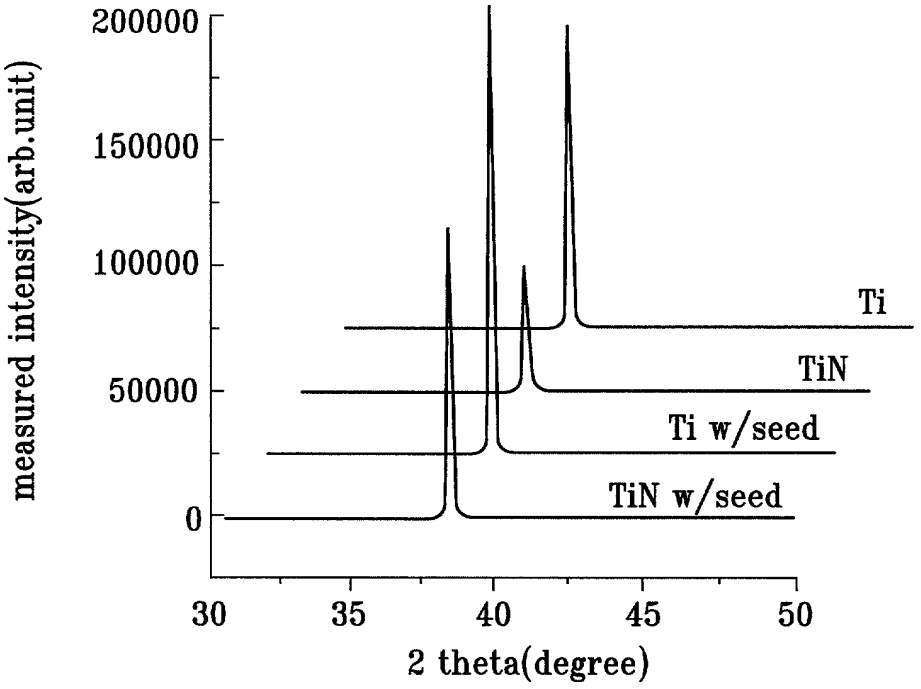

200000
150000
100000
50000
0
measured intensity(arb.unit)
Ti
TiN
Ti w/seed
TiN w/seed
30
35
40
45
50
2 theta(degree)

FIG.9b

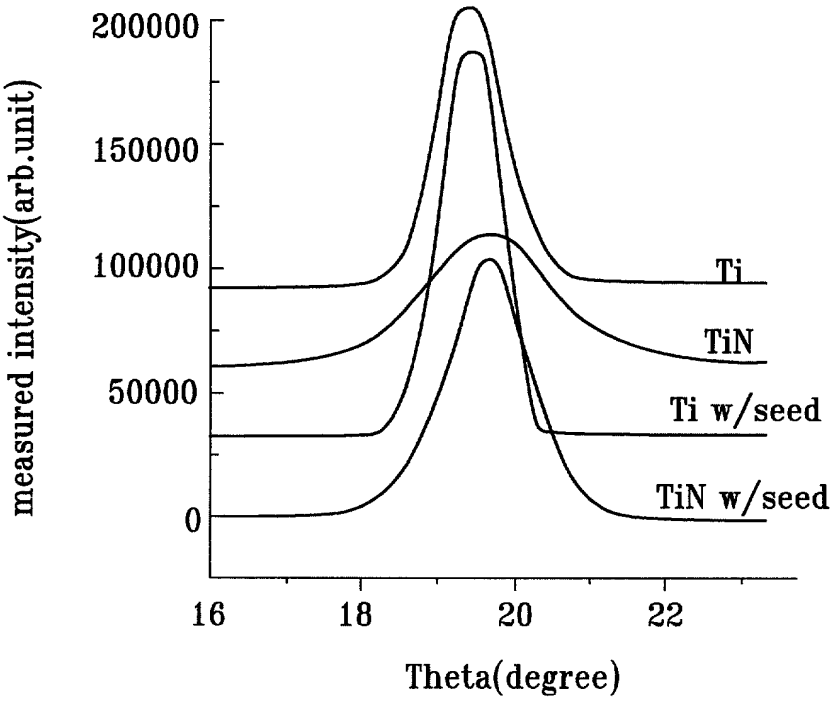

200000
150000
100000
50000
0
measured intensity(arb.unit)
Ti
TiN
Ti w/seed
TiN w/seed
16
18
20
22
Theta(degree)

FIG.10a

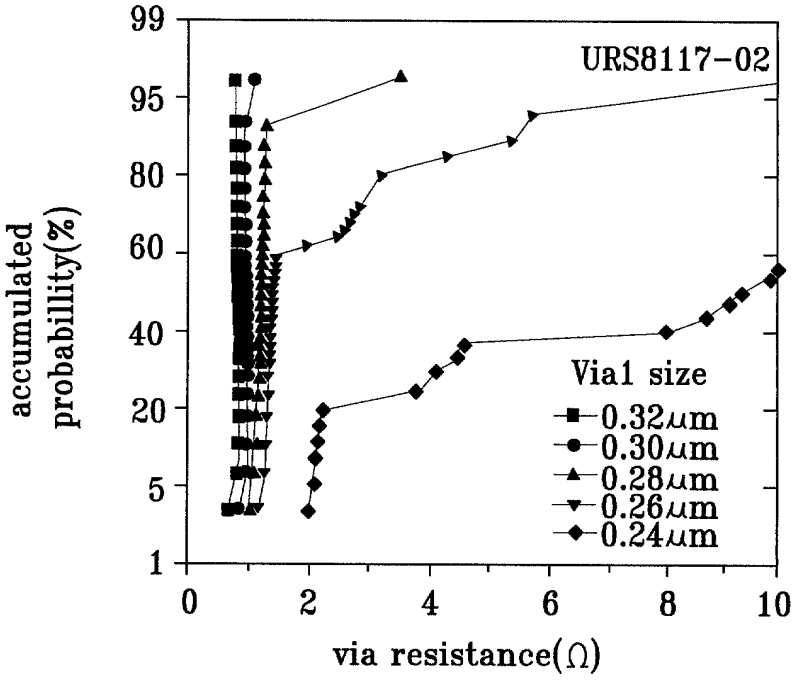


FIG.10b

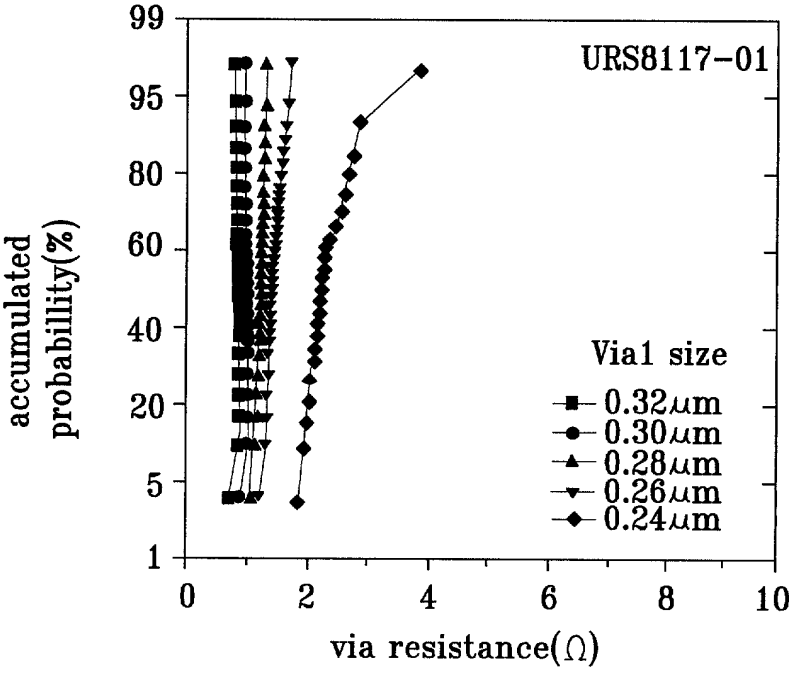


FIG.10c

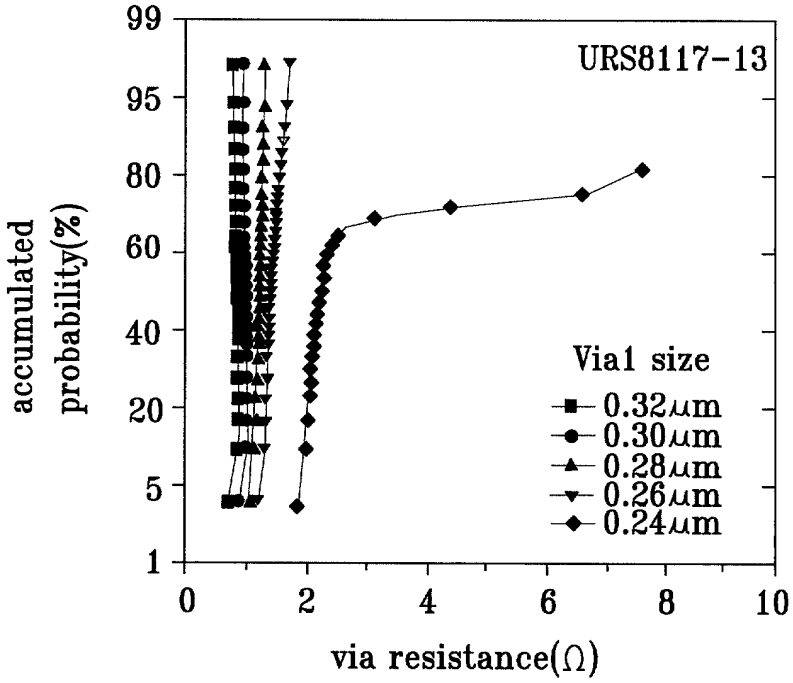
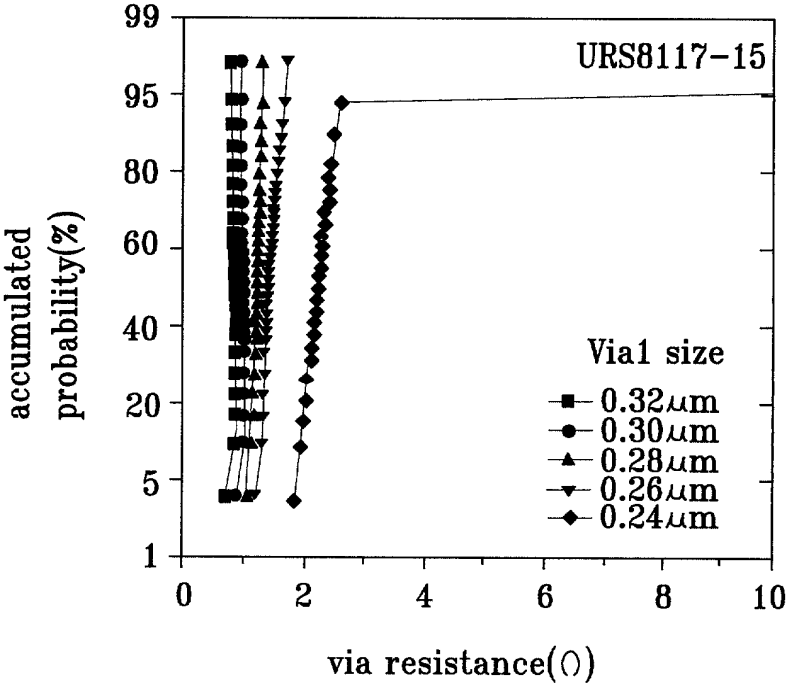


FIG.10d



COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

U.S. DEPARTMENT OF COMMERCE

Patent and Trademark

ATTORNEY DOCKET NO.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitle

METAL THIN FILM OF SEMICONDUCTOR DEVICE AND METHOD FOR FORMING SAME

the specification of which:

is attached hereto; or

was filed as United States application Serial No. _____ on _____ and was amended on _____(if applicable); or

was filed as PCT international application Number _____ on _____ and was amended under PCT Article 19 on_____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office information which is material to the patentability of claims presented in this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. §119:

COUNTRY (if PCT, indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C ¶119
Korea	42158/2000	July 22, 2000	[X] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

Combined Declaration For Patent Application and Power of Attorney - **(Continued)**
(includes Reference to PCT International Applications)

ATTORNEY DOCKET NO.:

I hereby claim the benefits under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

U.S. PROVISIONAL APPLICATIONS

U.S. PROVISIONAL APPLICATION NO.	U.S. FILING DATE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or §365(c) of any PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of claims presented in this application in accordance with Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT:

U.S. APPLICATIONS		STATUS (Check One)		
U.S. APPLICATION NO.	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

POWER OF ATTORNEY: As a named inventor, I hereby appoint the registered practitioners of Morgan, Lewis & Bockius LLP included in the Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that Customer Number.

Customer Number: 009629

Direct Telephone Calls To:
(name and telephone number)

Combined Declaration For Patent Application and Power of Attorney - **(Continued)**
(includes Reference to PCT International Applications)

ATTORNEY DOCKET NO.:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	Won Jun LEE	
RESIDENCE & CITIZENSHIP	Seoul, Korea	COUNTRY OF CITIZENSHIP Republic of Korea
POST OFFICE ADDRESS	Jinjoo APT., 4-410, 174-11, Yomni-dong, Mapo-ku, Seoul, Korea	
FIRST OR SOLE INVENTOR'S SIGNATURE	Won Jun Lee	DATE November 1, 2000
FULL NAME OF SECOND INVENTOR		
RESIDENCE & CITIZENSHIP		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		
SECOND INVEN TOR'S SIGNATURE		DATE
FULL NAME OF THIRD INVENTOR		
RESIDENCE & CITIZENSHIP		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		
THIRD INVENTOR'S SIGNATURE		DATE

Listing of Inventors Continued on attached page(s) [ ]Yes [X] No